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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,399	09/18/2003	Michael S. Leung	P0298US-7	8955

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EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

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05/11/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/666,399	LEUNG ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-33 and 35-46* is/are pending in the application.

4a) Of the above claim(s) *1-12,20-33 and 35-41* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,15-19 and 42-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/29/10, 4/09/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 22, 2010, has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 46 is rejected under 35 U.S.C. 102(b) as being anticipated by Mitchell et al. (US 5,766,987; hereinafter, Mitchell).

Regarding claim 46, Mitchell discloses a method (Figs. 3-5) for coating a plurality of semiconductor devices, comprising:

providing a mold (10, 32, Fig. 3) with a formation cavity (90, Fig. 5) for holding a plurality of semiconductor devices (50), said formation cavity (90) at least partially defined by opposing rigid upper (32) and lower (10) sections of the mold (col. 8, lns. 16-18);

mounting the plurality of semiconductor devices (50, Fig. 3) within said mold formation cavity to the lower section (10) with a film (52) between said semiconductor devices (50) and said lower section (10; col. 6, lns. 48-51), each of said semiconductor devices (50) being separately mounted in a pattern within the formation cavity (col. 7, lines 21-26 and 52-55), and provided with a space (72, Fig. 4; col. 7, lines 7-10) between respective tops (62) of said semiconductor devices (50) and said rigid upper section (32) to receive a curable coating material (51) (col. 8, lines 59-63);

injecting or otherwise introducing said curable coating material (51, Fig. 5; col. 8, lns. 59-63; col. 9, lns. 5-18) into said mold to fill said mold formation cavity (90, Fig. 5) and at least partially covering said semiconductor devices (50, Fig. 5) with coating material (51) and contacting said film (52, 84, Fig. 5; col. 8, lns. 61-62); and

curing or otherwise treating said coating material (51, Fig. 5; col. 9, lns. 33-45) so that said semiconductor devices (50, Fig. 3) are at least partially embedded in said cured coating material (51); and

removing said cured or treated coating material (51, Fig. 5) with said embedded semiconductor devices (50) from said formation cavity by releasing said film (52, col. 7, lns. 11-15) and said upper and lower sections (32 and 10) from said coating material and said semiconductor devices (50) leaving said coating material uncovered (col. 8, lns. 60-63; col. 9, lns. 48-53).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 13, 15-19 and 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitchell ('987; cited above) in view of Durocher et al. (US 6,614,103; hereinafter, Durocher).

Regarding claim 13, Mitchell discloses a method (Figs. 3-5) for coating a plurality of semiconductor devices, comprising:

providing a mold (10, 32, Fig. 3), with a formation cavity (90, Fig. 5) for holding a plurality of semiconductor devices (50), said formation cavity (90) at least partially defined by opposing rigid upper (32) and lower (10) sections of the mold (col. 8, lns. 16-18);

mounting the plurality of semiconductor devices (50, Fig. 3) within said mold formation cavity to the lower section (10), with a film (52 and 84) between said

semiconductor devices (50) and said upper and lower sections (32 and 10; col. 6, lns. 48-55), each of said semiconductor devices (50) being separately mounted in a pattern (col. 7, lns. 50-55) within the formation cavity;

injecting or otherwise introducing curable coating material (51, Fig. 5; col. 8, lns. 59-63; col. 9, lns. 5-18) into said mold to fill said mold formation cavity (90, Fig. 5) and at least partially covering said semiconductor devices (50, Fig. 5) with coating material (51) and contacting said film (52, 84, Fig. 5; col. 8, lns. 61-62); and

curing or otherwise treating said coating material (51, Fig. 5; col. 9, lns. 33-45) so that said semiconductor devices (50, Fig. 3) are at least partially embedded in said cured coating material (51); and

removing said cured or treated coating material (51, Fig. 5) with said embedded semiconductor devices (50) from said formation cavity by releasing said film (52, col. 7, lns. 11-15) and said upper and lower sections (32 and 10) from said coating material and said semiconductor devices (50) leaving said coating material uncovered (col. 8, lns. 60-63; col. 9, lns. 48-53).

Thus, Mitchell discloses all the limitations of the claim with the exception of disclosing wherein said curable coating material comprising at least one phosphor. However, Durocher discloses a method of packaging semiconductor devices (Fig. 3-13) wherein the semiconductor devices are light emitting diodes (59, Fig. 9) which are encapsulated by a curable coating material (65) comprising at least one phosphor (col. 8, lines 47-60), which converts one wavelength of LED radiation into another wavelength(s). Therefore it would have been obvious to one of ordinary skill in the art

at the time of the invention to incorporate the teaching of Durocher into the invention of Mitchell, to have the semiconductor chips (56) of Mitchell comprise light emitting diodes and the curable coating material comprise at least one phosphor, for the purpose of forming a light emitting diode (LED) array which is capable of producing white light or any other desired color (Durocher: col. 8, lines 49-60).

Regarding claim 15, Mitchell discloses the method further comprising separating said embedded semiconductor devices so that each is at least partially covered by a layer of said cured or treated coating material (col. 9, lns. 49-56).

Regarding claims 16, Mitchell discloses the method wherein said upper and lower sections (32 and 10, Fig. 4) provide opposing parallel surface, said semiconductor devices (50) arranged on one or both of said opposing surfaces (14, Fig. 3).

Regarding claims 17, Mitchell discloses the method claim wherein said curing or otherwise treating said coating material comprises one of the methods from the group comprising heat curing, optical curing or room temperature curing (col. 9, lns. 32-39).

Regarding claim 18, Mitchell discloses the method wherein the semiconductor devices are separated by dicing or scribe and break (col. 9, lns. 51-54).

Regarding claim 19, Mitchell discloses the method wherein the semiconductor devices are separated such that the layer of cured or otherwise treated coating material conforms to the shape of the semiconductor device (col. 9, lns. 38-56).

Regarding claims 42 and 43, Durocher discloses a plurality of semiconductor devices comprise light emitting diodes (59, Fig. 9) and a curable coating material (65) comprises a matrix material containing light conversion particles (col. 8, lines 47-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to incorporate the teaching of Durocher into the invention of Mitchell, for the same reasons as set forth above.

Regarding claim 44, Mitchell discloses wherein said plurality of semiconductor devices comprising contacts with one of said contacts (64, Fig. 4) covered by said film (84, Fig. 4).

Regarding claim 45, Mitchell discloses wherein said removing the cured or treated coating material with the embedded semiconductor devices by releasing said film leaves said contacts uncovered by said coating material (col. 9, lns. 49-51: it is implicit that once top cover layer 84 is removed, the contacts will be exposed).

Response to Arguments

4. Applicant's arguments regarding claims 13, 15-19 and 42-45 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claim 46, Applicant argues:

> Mitchell teaches "the top fixture element 32 bears on the terminals 64 and dielectric layers 60 of the subassemblies through the top covering layer 84" (col. 8, lns. 6-9) to "prevent contamination of terminal 64" (col. 9, lns 10-12) with the encapsulant. No space is taught between the subassemblies and the top fixture element 32 "to receive a curable coating material."

The argument is not persuasive. As set forth in the rejection above, Mitchell clearly discloses a space (72, Fig. 4; col. 7, lines 7-10) between respective tops (62) of said semiconductor devices (50) and said rigid upper section (32) to receive a curable coating material (51) (col. 8, lines 59-63);

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Wael M Fahmy/
Supervisory Patent Examiner, Art Unit 2814